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ALTIUMLIVE: PCB DESIGN VS PRODUCT DESIGN: UNLEASHING THE POWER OF EFFECTIVE MULTI-BOARD DESIGN



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Multi-Board Challenges

Multi-Board in Altium Designer

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Resolving Challenges

How do you manage...

- I. System Level Design Strategies
- II. Form & Fit
- III. Connectors and Connections



System Level Design Strategies

In any system level solution, we look for

- 1. Definition (what),
- 2. Collaboration (who),
- 3. and Tools (how).



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So, let's look at WHAT first:

Many connectors are dual sourced. Meaning, two companies are responsible for the manufacturing of each mating part of the connection.

Examples of these are:

- Edge Connectors
- Wires
- Memory Chip Connectors (SD or PC)



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Alignment and Orientation becomes difficult to manage.

Even single source connector systems have challenges with Alignment and Orientation.







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Hirose B2B connector

WHO? Collaboration involves many different perspectives.

The EE wants to show the signal coming in &/or going out from each source.



The ME wants to position the connector(s) so they are accessible.





The Designer wants to be sure the correct signal is going through the correct connector and how best to swap pins to ease routing complexity.



Form and Fit

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The display's background is normally black, but changes to orange when heating and blue when cooling.



To track the Mechanical placement and clearances we use:

2D DFX files generated from one CAD program and imported another.



These require other additional pieces of data supplied by emails &/or pictures for heights and dimensions.

Form and Fit

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Or we can import Mechanical placement and clearances using 3D STEP files:

These files are generated first from the MCAD software and imported into the ECAD software.

Then a STEP file is generated from the ECAD software and imported to into the MCAD software.



There are many issues with this process:

- 1. Alignment and Orientation are often different in each CAD package.
- 2. For connectors, the signals DO NOT Translate in this process.
- 3. Connector naming schemes are not coordinated or thought out.

Connectivity Management

Pin Swapping

Synchronizing Nets Across Boards

Matching and Mirroring

Commonly managed with XLS or DOC files and Emails!

			NB2DSK-J15-3	SPK.SPK_R+	SPK01-HDR1-3	R_PLUS
			NB2DSK-J15-4	SPK.SPK_R-	SPK01-HDR1-4	R_MINUS
			NB2DSK-J15-5	GND	SPK01-HDR1-5	GND
			NB2DSK-J15-6	5V0	SPK01-HDR1-6	5V0
			NB2DSK-J15-7	SPK.SPK_L-	SPK01-HDR1-7	L_MINUS
			NB2DSK-J15-8	SPK.SPK_L+	SPK01-HDR1-8	L_PLUS
			NB2DSK-J15-9	EXTCTRL#.DIN2	SPK01-HDR1-9	DIN2
			NB2DSK-J15-10	EXTCTRL#.SCK2	SPK01-HDR1-10	SCLK2
	_		NB2DSK-J15-11	EXTCTRL#.CS1_N	SPK01-HDR1-11	CS1_N
	_		NB2DSK-J15-12	EXTCTRL#.CS2_N	SPK01-HDR1-12	CS2_N
			NB2DSK-J15-13	EXTCTRL#.DIN1	SPK01-HDR1-13	DIN1
			NB2DSK-J15-14	EXTCTRL#.1WIRE	SPK01-HDR1-14	ONE_WIRE
			NB2DSK-J15-15	EXTCTRL#.SCK1	SPK01-HDR1-15	SCLK1
			NB2DSK-J15-16	3V3	SPK01-HDR1-16	3V3
	nnection	Name: Direct (C_2)				
	1		DaughterBoard-HDR_L1-1	EXTEND_A0	NB2DSK-HDR_L1-1	EXT_A.D0
	2		DaughterBoard-HDR_L1-2	EXTEND_B0	NB2DSK-HDR_L1-2	EXT_B.D0
2	3		DaughterBoard-HDR_L1-3	EXTEND_A1	NB2DSK-HDR_L1-3	EXT_A.D1
23	4		DaughterBoard-HDR_L1-4	EXTEND_B1	NB2DSK-HDR_L1-4	EXT_B.D1



Connectors and Connections

Today's TOOLS are many and separate. To track the Electrical properties of signal flow & logic we use:



Pinout Diagrams,



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Excel spread sheets



Wiring Diagrams



Connectivity Management starts with identification.

The IPC-7X51 (NEMA & MIL SPEC) have a naming conventions for Connectors and Mechanical Components. These are all very basic and specific to the Manufacturer of the connector. Mostly they consists of (IPC shown):

abbreviation for Manufacturer's Name (e.g. 3M, DEGSON, HARWIN...) + _
(underscore) + Manufacturer's Part Number (Manufacturer's Code).

These don't quite go far enough for our purposes....

We have to know which connector mates with what other connector?

To do this we have two reference designators: "J" & "P".

These are a matching, Androgynes pair!

Their individual NUMBER then helps us to identify who goes with who:



J100 – P100 J101 – P101 J102 – P102 Etc.

Now we are set to do some Pin Swapping and Signal (NET) management!

System Level Architecture

Edit boards in a system context

Verify system level connectivity on the logical and physical side

System Context Outside of Design Environment



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Multi-Board Challenges

- Multi-Board in Altium Designer
- Resolving Challenges

Design Methodology

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- Logical System-Level Design
- Electrical Rules Check
- Connection Management
- Assembly Creation
- Single Editing Environment
- Physical Assembly Optimization

Create logical design interconnections between modules

Module represents a complete printed circuit board project with all associated files



Connection Violations

Mated Part Violations

Optio	ns for Multi-board Design Project MiniPC.PrjMbd	×
Error Reporting Parameters Server Parameters		
Violation Type Description	Report Mode	
 Violations Associated with Connections 		
Different Net Names	📁 Fatal Error	
No Net	🖿 No Report	
Unresolved Conflict	🖿 No Report	
 Violations Associated with Mated Parts 		
Entry Is Empty	No Report	
No Mated Part	No Report	
Report Suppressed Violations in Messages Panel		
Set To Installation <u>D</u> efaults		K Cancel

Connection Management

Direct Connection: Direct contact between boards.

Wire: A single wire connecting two points across boards.

Cable: An inseparable bundle of wires used to connect boards.

Harness: A collection of cables and wires connected two or more points across two or more boards.



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Connection Manager

Track signals across each PCB layout

Conflict Resolution

Validate pin swaps and connectivity changes across designs to ensure acknowledgment of changes between teams

Confirm - Approves swapping without any changes

Revert - Cancels changes in first child project and requires back ECO to complete changes

Swap Pins – Replicates changes in mated part.

ි Clipboard	Report Show Co	onnections Show Mate	ed Pins		
Vire		From			
D	Net Name	Pin	Module Net	Pin	Module Net
▲ Direct (C3)					
36	mini_PCIE_USB_D_N/PA1	M1-J13-36	mini_PCIE_USB_D_N	M4-P1-36	PA12_USB_D_P
38	mini_PCIE_USB_D_P/PA1	M1-J13-38	mini_PCIE_USB_D_P	M4-P1-38	PA12_USB_D_N
		Confli	ct Resolution		
M1	J13 Pin 38			P1 Pin 36	M4 Nets connected to Pin 36
Swap Pins	Pin 36			Pin 38	and Pin 38 were swapped

Physical connections between individual designs and enclosures

Navigate all assembly aspects

Track signal connectivity on a physical and logical level.



Visual verification of position and enclosure fit

Adjustable and X/Y/Z plane section cutout





Precise board alignment

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Two point, plane-to-plane, and axis-to-axis alignment



Move components on any selected board in the assembly

Changes sent to the original PCB design

Ensure relative position while allowing placement optimization

Measure distance between design aspects



Physical Assembly Optimization

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Orthographic View

Perspective View



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Multi-Board Challenges

Multi-Board in Altium Designer



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Resolving Challenges

Resolving Challenges



DEMO

- I. System Level Design Strategies
- \checkmark Logical System-Level Design
- \checkmark ECO Driven Design Synchronization
- \checkmark Visualizing Your Product's Interior



II. Form & Fit

- ✓ Assembly Hierarchy Navigation
- $\sqrt{Board Alignment}$
- √Optimized Part Placement



III. Connectors and Connections √Connection Definitions

- \checkmark Electrical Rule Check
- \checkmark Resolving Board Connectivity Conflicts



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