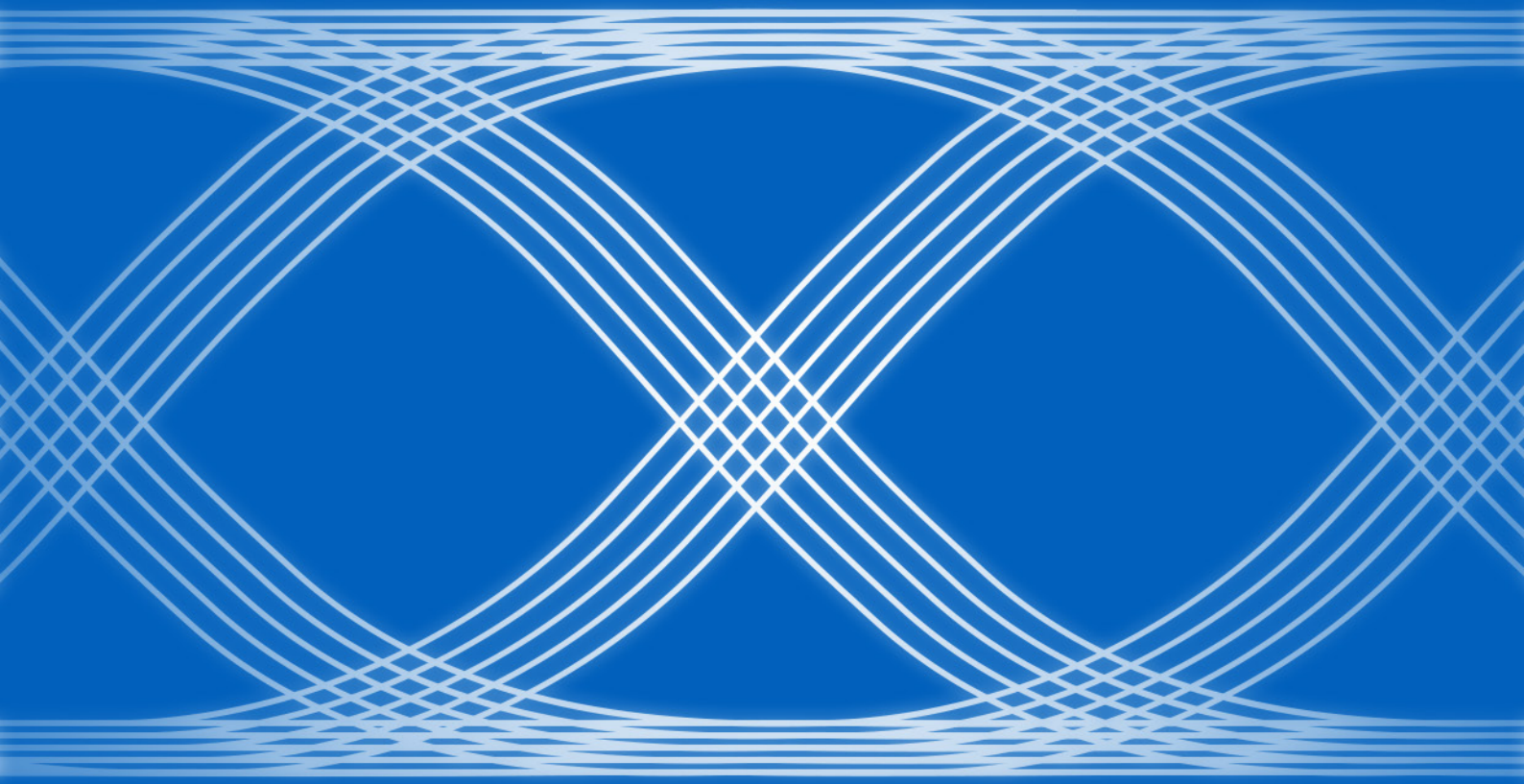
Altium

Adopting Signal Integrity in Your High-Speed Design Process



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INTRODUCTION - WHAT IS SIGNAL INTEGRITY?

Today's engineers will learn that signals are transmitted from an emitter to a receiver in an ideal way based on theories and ideal simulations, but real world applications often have their own surprises. The way signals operate in reality is often very different from the theoretical applications taught in universities, and as a consequence, moving from theory to practical application can often lead to unpredictable results.

When current goes through a copper trace, different behaviors may arise depending on the energy delivered by the driver of the source component (emitter). Signal Integrity simulation is an ideal way to verify the quality of a signal passed through a copper trace ensuring that the whole system is safe and functional. Signal Integrity analysis is a post-layout simulation process that accurately reflects what is happening in reality and what behaviors will occur in the daily use of a product, allowing you to more consistently design reliable products.

WHY SHOULD I WORRY?

The use of high-speed components has been increasing in the marketplace, while use of low-speed components continues to decline. This trend continues even today, and the rising use of high-speed components offers the challenge of maintaining signal quality in our complex systems.

A signal can be disturbed in a variety of ways, including losses, crosstalk effect, reflection, skin effect and many other perturbations. These signal disturbance issues are further complicated in technologies such as DDR 2/3/4, where every signal needs to arrive at the same time in order to be read from memory while maintaining the same clock speed.

Fast pin drivers are commonly utilized to achieve good timing on signals, while also delivering enough energy along the copper trace. While these pin drivers can help to minimize signal integrity loss, long transmission lines are subject to perturbations.

Some theoretical applications to be aware of:

The Transitional-Electrical-Length (TEL) is defined as the movement of an electromagnetic wave during a signal change (Rise Time (RT) / Fall Time (FT)):

- `TEL = RT/FT * Signal Velocity`

A Trace on a PCB build with FR-4 has an approximate velocity of:

- `15 cm/ns (6 inches/ns)`

With a Rise / Fall Time of e.g. `300 ps` this means:

- `TEL = 0,3 ns * 15 cm/ns = 4.5 cm (1.77 inches)`

If the Trace is longer than 20% of the TEL, we will get a Transmission Line and Reflections:

- `Reflection starts with = 0,3 ns * 15cm/ns * 0.2 = 9 mm (350 mil)`

What does this all amount to? Copper traces that are longer than 9mm (350mils) act like transmission lines and require special attention during your design process.

ANALYZING RISKS

Because there are different kinds of perturbations that can affect a copper trace, there are also several different risks and consequences to be aware of if you don't check the quality of the signal in your systems. For example, let's look at a reflection issue. The signal is sent from the emitter to the receiver, but some energy overflow is observed at the pin of the receiver as shown in **Figure 1** below.

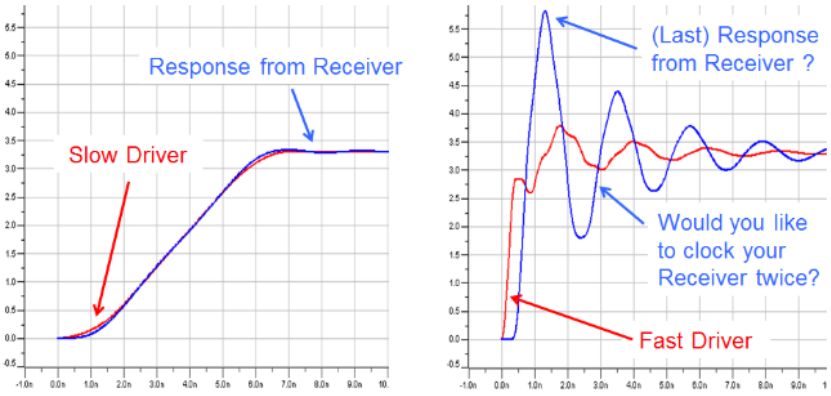

Figure 1 - Signal reflection issue from emitter to receiver

When observing this effect, we can see various distortions of the signal, like an overshoot that could burn the chip or an undershoot that could switch the device twice. In this second situation, we should also make note of the ring back, which might also switch the device again. In both cases the risks are high, and this signal quality issue will likely generate additional costs for prototypes and re-spins. It may even lead to some non-functional systems when the product is on the market. Beyond mere technical risks, there is also the impact on a company's budget to consider, as costs begin to spiral out of control with each round of prototypes that is made.

At its worst, problems not detected during the prototype phase will go to market with a number of bugs and issues still waiting to be discovered. And in a situation like this, you'll likely spend a large amount of resources repairing or replacing products when they are returned by your customers. And the last thing your company wants to deal with is a product being recalled, damaging your brand's reputation and budget in the process.

POSSIBLE SOLUTIONS

How can we avoid signal integrity issues and save ourselves from all of these potential problems? The first step is to thoroughly research the issue you encounter from the beginning and make good design decisions throughout your design process. In other words, don't go diving in without a concrete plan for success in place.

What should your plan entail? The most common approach is to adapt the impedance of the transmission line. This requires an impedance controlled routing. If you need a bigger adaptation, a termination can be added to the signal. This will also adjust the impedance, allowing you to avoid traces that are too wide on the PCB. By doing this, the termination component absorbs energy overflow on the transmission line, thus protecting your receiver.

Another key factor to avoid perturbations is to plan out your current return path. Avoid splitting power planes in the area below (or above) critical signals. Also make use of blind and buried vias for these critical signals, as stubs of through hole vias might act as an antenna and will generate unwanted perturbations on the signal.

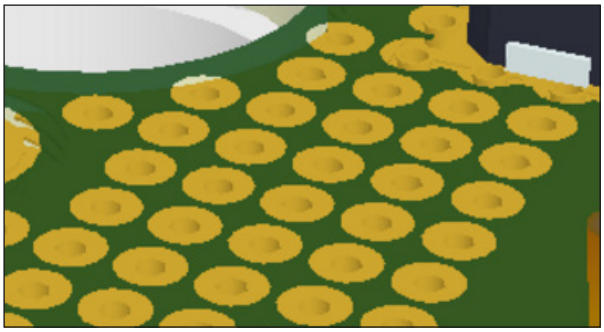

Figure 2 - Via Stitching made by Altium Designer to provide an optimized current return path

HOW CAN ALTIUM DESIGNER HELP YOU?

Altium Designer includes a complete signal integrity analysis tool that can help you to detect perturbations and distortions of the signals on your board. First, it contains a pre-layout analysis that makes an estimation of the problems that might happen on your project. This is helpful when it comes to detecting problems with signals early in the design process and making better decisions when it comes time to make your layout. Of course, at this stage of the design, the analysis doesn't have information about the real layer stack and can only make estimations on the results. When the board is completed, with the routing and all copper areas, then the post-layout analysis can be utilized to see the real perturbations of the signals.

As usual, simulation models are required in order to run the simulation. In the case of a Signal Integrity simulation, IBIS models are required for all IC's connected to the signals we want to simulate. Altium Designer can manage the IBIS models for basic components, such as resistors, capacitors, inductors, connectors, transistors, diodes and more... The only things you need to concern yourself with are the simulation models for the IC's. These can typically be downloaded from the manufacturer's website.

With the routing on the board and the IBIS models attached to your components, you can now start the Signal Integrity simulation. Run the analysis and investigate the quality of your signal. If you see unexpected perturbations, then you'll want to run the simulation again. This time, use a variation of the possible terminations that can be added to the signal. Altium Designer will generate signals with these terminations on the same chart so that you can understand what kind of termination is required to adjust the critical signal.

Now that you know which termination you need, you can also run an additional analysis, to determine what value you need for your component so you can make the best adaptation for the signals. This is a parametric simulation that can vary the value of the termination component, allowing you to see which value will help the most.

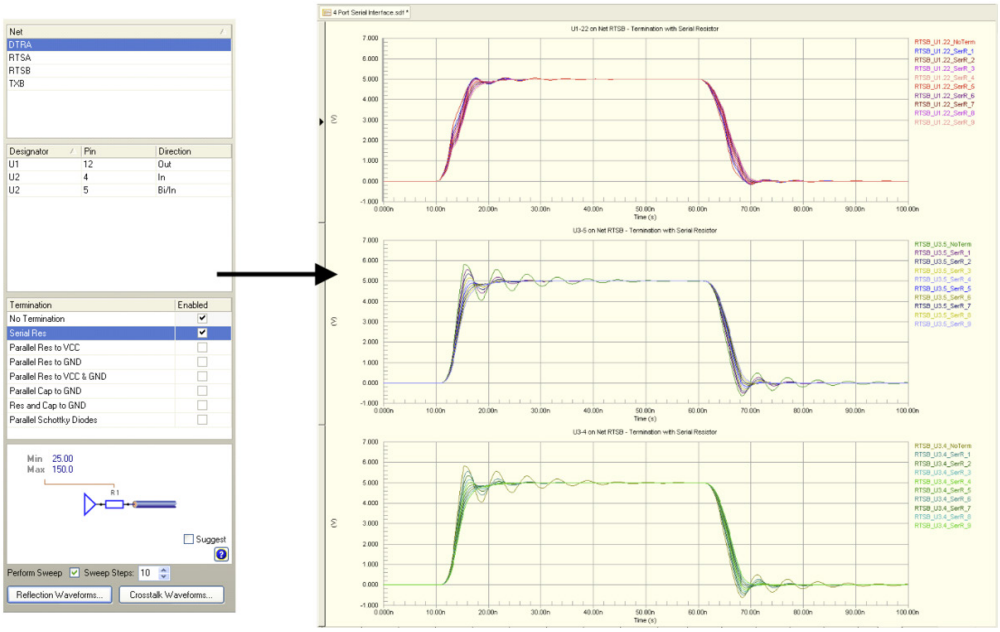

Figure 3 - Parametric simulation of a pull down resistor termination

CONCLUSION

With the help of Signal Integrity simulation in Altium Designer, it can be easy to successfully navigate the intricacies of your high-speed board both before and after your routing process. But it's not all about the simulation tool, and you'll want to spend an ample amount of time planning your current return path, signal timing, and layer stackup before you ever start routing traces. With a combination of post and pre-layout simulation and careful planning, you'll be able to produce a clear signal every time.